In the Specification

Please amend Page 6, lines 7-11, as follows:

Figure 16 illustrates pipeline and program memory busses for near-by memory, program memory and accesses according to the concepts of the present invention; ~~and~~

Figure 17 illustrates pipeline and program memory busses for near-by memory for an interrupt taken in place of executing instruction I2 according to the concepts of the present invention.; and

Figure 18 illustrates a block diagram for generating addresses for various accesses according to the concepts of the present invention.

In the Specification

Please amend Page 26, lines 14-17, as follows:

If the information is of the data type, the information will go on PMD bus, through the data multiplexer **175**, to be input to register **180**. The data multiplexer **175** is controlled by the decoding of the address for a read transaction so that the source of the data is properly selected from either a distant or near by memory block.